REMARKS

Present Status of the Application

The Office Action rejected claims 9-14 under 35 U.S.C. 103(a), as being unpatentable over Komatsu (U.S. 6,380,053; hereafter Komatsu) in view of Liaw (U.S. 6,448,140; hereafter Liaw). Applicant respectfully traverses the rejection but has amended claim 9 to improve clarity. Furthermore, Application has added claims 15-17 for re-defining the present invention. No new matter has been introduced into the application by the amendment made herein. After entry of the foregoing amendments, claims 9-17 remain pending in the present application, and reconsideration of those claims is respectfully requested.

Discussion of Office Action Rejections

The Office Action rejected claims 9-14 under 35 U.S.C. 103(a), as being unpatentable over Komatsu (U.S. 6,380,053) in view of Liaw (U.S. 6,448,140).

Applicant respectfully traverses this rejection and submits that Komatsu in view of Liaw is legally deficient to render claim 9 unpatentable. As stated claim 9 recites:

> Claim 9. A semiconductor device, comprising:
> a substrate;
> a gate structure on said substrate, said gate structure including a gate dielectric layer on said substrate and a gate conductive layer on said gate dielectric layer;
> an oxide spacer on a sidewall of said gate structure;
> a spacer on said oxide spacer;
> a source/drain region in said substrate besides said gate structure and said spacer; and
> an offset oxide layer on said substrate and in a portion of said source/drain region, wherein said offset oxide layer having a bottom surface below a bottom surface of said gate dielectric layer is apart from said gate structure and adjacent to said spacer.

(*Emphasis Added*) Applicants submit that the claim patently defines over the prior art of record, for at least the reason that the prior arts fail to disclose at least these elements emphasized above.

In the present invention, as shown in Fig. 1F, the semiconductor device possesses an offset oxide layer 124 in the substrate adjacent to a portion of the substrate covered by the spacer 120 and apart from the gate structure. More specifically, the bottom surface of the offset oxide layer is lower than the bottom surface of the gate dielectric layer of the gate structure. On the other words, the offset oxide layer 124 is an extension portion of the oxide layer 112 which is located between the gate structure and the spacer 120 and between the spacer 120 and the substrate 100. It should be noticed that the thickness of the offset oxide layer 124 is larger than that of the oxide layer 112.

However, Komatsu fails to teach or suggest that the silicon oxide layer (as shown in Fig. 3 of Komatsu's application) is substantially apart from the gate structure. Instead, Komatsu emphasizes that the formation of the silicon oxide layer, which is partially transformed by oxidizing the sidewall of the polysilicon layer 21A, is the claimed feature of his application (col. 9, lines 27-40). Because of silicon oxide layer, the thickness of the gate insulating layer 20 in the vicinity of the side wall of the gate electrode 21 can be increased and as a result, an overlap capacitance between the marginal portion of the gate electrode 21 and the source/drain region 23 can be decreased. That is, Komatsu emphasizes that the advantages of his application is achieved by oxidizing the sidewall of the polysilicon layer 21A to form the silicon oxide layer after the sidewalls 22 is removed. Apparently, the silicon oxide layer disclosed by Komatsu must be

located at the substrate directly adjacent to the gate structure and partial of the silicon oxide layer is transformed from the sidewall of the polysilicon layer 21A.

Hence, even if skilled artisan modified Komatsu by referring to Liaw, the result device structure is still different from what claimed by the present invention. Additionally, in the cited art, the formation of the silicon oxide layer leads to the loss of the sidewall of the polysilicon layer 21A. Hence, the electrical performance of the gate electrode with the polysilicon layer 21A of which the sidewall is oxidized is quit different from that of the gate electrode of which the sidewall is covered by the spacer without being oxidized.

Hence, Applicants respectfully submit that Komatsu in view of Liaw fails to render claim 9 obvious. Claims 10-14, which depend from claim 9, are also patentable over Komatsu in view of Liaw, at least because of their dependency from an allowable base claim. Applicants respectfully assert that these claims are in condition for allowance. Thus, reconsideration and withdrawal of this rejection are respectively requested.

Newly Added Claims

Applicant has added claims 15-17 for defining the present invention by introducing that the offset oxide layer is located in the heavily doped region and apart from the gate structure. It is believed that no new matter is introduced into the application by adding the new set of claims.

As the same reasons discussed above for the rejection 103, Applicant respectfully submits that the combination of cited arts does not render claims 15-17 unpatentable.

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CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims 9-14 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,
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